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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,941	01/16/2004	Charles Ray Johns	AUS920030429US1	8208

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EXAMINER	
KROFCHECK, MICHAEL C	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,941	JOHNS ET AL.	
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,12-16 and 25-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,12-16 and 25-39* is/are rejected.

7)☐ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on 6/8/2006.

2. Claims 1-5, and 12-16 have been amended.

3. Claims 6-11 and 17-24 have been cancelled.

4. Claims 25-39 have been added and examined.

5. The objections/rejections from the prior correspondence not restated herein have been withdrawn.

Claim Objections

6. Claim 5 is objected to because of the following informalities:

a. In light of the amendments to claims 4-5, and 15-16, the examiner believes the applicant intended to state, "wherein the ***management device*** manages the pre-load unit."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 1-5, 12-16 rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA), Hammond, US patent 5918250, and Saxena, US patent 5699543.

11. With respect to claim 1, AAPA teaches of an apparatus for managing a translation mechanism in a processor architecture comprising: an execution unit for generating an effective address (fig. 1-2, items 110, 210; page 5, lines 22-26, page 6, lines 2-6; where the execution unit issues effective addresses (EA));

a translator coupled to the execution unit, wherein the translator translates the effective address into a real address utilizing the translation lookaside buffer (fig. 1-2, items 112, 212; page 5, line 26-page 6, line 4; page 6, lines 18-23; where the TLB searches for a translation (real address) for the EA);

a storage device, wherein the storage device stores general data and wherein the general data is referenced by the real address (fig. 1-2, item 116, 216; page 5, lines 16-17, 24-page 6, line 7; The EA references to data in the main storage are translated into real addresses (RA), this is done because the data in the main storage is referenced by the RA and not the EA)

AAPA fails to explicitly teach of a pre-load unit that loads translation data into a translation lookaside buffer, for at least one translation of at least one effective address into at least one corresponding real address, prior to execution of an application corresponding to the at least one translation.

However, Hammond teaches of a pre-load unit that loads translation data into a translation lookaside buffer, for at least one translation of at least one effective address into at least one corresponding real address (fig. 1; items 197, 195; column 4, line 58-column 5, line 15; where the preload circuit preloads the translation attribute data and if it matches, the software TLB handler only needs to load one register).

Saxena additionally teaches of a pre-load unit that loads translation data into a translation lookaside buffer, for at least one translation of at least one effective address into at least one corresponding real address, prior to execution of an application corresponding to the at least one translation (fig. 6; column 4, lines 49-65);

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA and Hammond at the time of the invention to include the preload circuit, software TLB handler, and the means to use them as taught in Hammond in AAPA. Their motivation would have been to decrease the time for a TLB fill and make the process as streamlined as possible (Hammond, column 2, lines 28-31).

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Hammond, and Saxena at the time of the invention to include the process of preload the TLB translations for the working pages of a program in the combination of AAPA and Hammond as taught in Saxena. Their motivation would have been to redle the number of TLB misses and improve system efficiency (Saxena, column 1, lines 35-41).

12. With respect to claim 12, AAPA teaches of a method for managing a translation mechanism in a processor architecture comprising: generating an effective address (fig. 1-2, page 5, lines 22-26, page 6, lines 2-6; where the execution unit issues effective addresses (EA));

translating the effective address into a real address utilizing the translation lookaside buffer (fig. 1-2; page 5, line 26-page 6, line 4; page 6, lines 18-23; where the TLB searches for a translation (real address) for the EA);

accessing stored general data in a storage device based on the real address (fig. 1-2, item 116, 216; page 5, lines 16-17, 24-page 6, line 7; The EA references to data in the main storage are translated into real addresses (RA), this is done because the data

in the main storage is referenced by the RA and not the EA. It is abundantly clear to one of ordinary skill in the art that this is done to access the data in the main storage).

AAPA fails to explicitly teach of pre-loading translation data into a translation lookaside buffer, for at least one translation of at least one effective address to at least one corresponding real address, prior to execution of an application corresponding to the at least one translation;

However, Hammond teaches of pre-loading translation data into a translation lookaside buffer, for at least one translation of at least one effective address to at least one corresponding real address (fig. 1; items 197, 195; column 4, line 58-column 5, line 15; where the preload circuit preloads the translation attribute data and if it matches, the software TLB handler only needs to load one register)

Saxena additionally teaches of pre-loading translation data into a translation lookaside buffer, for at least one translation of at least one effective address to at least one corresponding real address, prior to execution of an application corresponding to the at least one translation (fig. 6; column 4, lines 49-65).

13. With respect to claim 2, AAPA teaches of wherein the storage device further comprises a page table (fig. 1-2, item 118, 218), and wherein the page table is configured to provide a reference to the general data (fig. 1-2; page 6, lines 3-7; the miss handler searches the page table for the translation to translate the EA, thus the page table references the data in the storage through the EAs and RAs addressing that data).

14. With respect to claim 13, AAPA teaches of the step of accessing further comprises accessing a page table, and wherein the page table is configured to provide a reference to the general data (fig. 1-2; page 6, lines 3-7; the miss handler searches the page table for the translation (RA) to translate the EA. The RA references the data and thus the page table references the data in the storage through the EAs and RAs addressing that data).

15. With respect to claims 3 and 14, Hammond teaches of wherein the pre-load unit further comprises a communication channel between the page table and the translator (fig. 1; column 1, lines 24-26; where the memory management unit (translator) translates the virtual address into its physical address using the page tables. Since the MMU must communicate with the page table to do such, there must be a channel of communication between them).

16. With respect to claims 4 and 15, AAPA teaches of wherein the translation mechanism further comprises a management device, provided as one of a software manager or a hardware manager, coupled to the translator (fig. 1, item 102; page 5, lines 9-12; page 6, lines 9-11).

17. With respect to claims 5 and 16, the combination of AAPA, Hammond, and Saxena teaches of the step of utilizing the management device further comprises: transporting data through a data port between a pre-load unit, that performs preloading of translation data, and the translation lookaside buffer (AAPA, page 8, lines 5-6, It is abundantly clear to one of ordinary skill in the art that in the combination of AAPA, Hammond, and Saxena, the data port is located between the TLB and the hardware

running the optimizer of Saxena, as communication between the two is required in order preload the translations); and

supplying index data from an index table to the translator (AAPA, page 8, lines 8-12),

wherein the management device manages the pre-load unit (Saxena, fig. 1-2, 6; column 3, lines 11-13, lines 21-27, column 4, lines 49-65; it is abundantly clear to one of ordinary skill in the art that the hardware running the optimizer is controlled by the optimizer).

18. With respect to claims 25 and 30, the combination of AAPA, Hammond, and Saxena teaches of wherein the pre-load unit loads a plurality of translations into the translation lookaside buffer based on a page table associated with the storage device prior to execution of the application (Saxena; fig. 3, column 3, line 29-column 4, line 8; where the preloaded translations are based on the pages needed for the application. as the application is read from disk into the memory, the pages are associated with the disk).

19. Claims 26-27 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hammond, and Saxena as applied to claims 25 and 30 respectively, and further in view of Thaler et al., US patent 5983329.

20. With respect to claims 26 and 31, Thaler teaches of a read/write request that identifies the desired read/write area by an effective start address and a region size parameter (column 6, lines 39-48).

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Hammond, Saxena, and Thaler at the time of the invention to identify the translations to be preloaded from the page table in the combination of AAPA, Hammond, and Saxena in the manner that Thaler identifies the data to be read or written. Their motivation would have been to provide a quick, simple, generalized way of identifying the group data entries to be copied, and avoiding the need to individually identify each entry.

21. With respect to claims 27 and 32, the combination of AAPA, Hammond, Saxena, and Thaler teach of the limitations of claims 26 and 31 as cited above. The application, on page 12, line 18-21, defines the madvise call to have an effective address and region size parameter, which is the same as in claims 26 and 31.

22. Claims 28-29 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hammond, and Saxena as applied to claims 25 and 30 respectively, and further in view of Aglietti et al., US patent 6766435.

23. With respect to claims 28-29 and 33-34, Aglietti teaches of storing a state of the translation lookaside buffer in response to a swap of tasks from a first task to a second task running on the execution unit and restoring a state of the of the translation lookaside buffer in response to a swap of tasks from the second task to the first task running on the execution unit (abstract and column 5, lines 18-26; where in response to a context switch the address translation information is stored and then restored the next time the process is executed).

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Hammond, Saxena and Aglietti at the time of the invention to store and restore the address translation information from the TLB in response to context switches in the combination of AAPA, Hammond, Saxena as taught in Aglietti. This would be done by the hardware executing the optimizer in the combination of AAPA, Hammond, Saxena. Their motivation would have been to eliminate the pollution of the TLB (Aglietti, column 1, lines 58-62).

24. Claims 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Hammond, Saxena, and Belair US patent 6212613.

25. With respect to claim 35, the combination of AAPA, Hammond, and Saxena teaches of the limitations of claims 1 and 12. Additionally, Belair teaches of, the computer program product having a medium with a readable computer program embodied thereon (fig. 1, item 28; column 5, lines 12-15; column 6, lines 36-43).

It would have been obvious to one of ordinary skill in the art having the teachings of AAPA, Hammond, and Saxena, and Belair at the time of the invention to include the programs/control code of the combination of AAPA, Hammond, and Saxena on a computer readable medium. Their motivation would have been to provide a way to input and potentially upgrade the code, Belair column 12, lines 43-51.

26. With respect to claim 36, the combination of the combination of AAPA, Hammond, Saxena and Belair, teach of the limitations of claim 36 as cited with respect to claims 2 and 13 above.

27. With respect to claim 37, the combination of the combination of AAPA, Hammond, Saxena and Belair, teach of the limitations of claim 37 as cited with respect to claims 3 and 14 above.

28. With respect to claim 38, the combination of the combination of AAPA, Hammond, Saxena and Belair, teach of the limitations of claim 38 as cited with respect to claims 4 and 15 above.

29. With respect to claim 39, the combination of the combination of AAPA, Hammond, Saxena and Belair, teach of the limitations of claim 39 as cited with respect to claims 5 and 16 above.

Response to Arguments

30. Applicant's arguments filed on 6/8/2006 have been fully considered but they are not persuasive.

31. Applicant's arguments with respect to claims 1-5, 12-16, and 25-39 have been considered but are moot in view of the new ground(s) of rejection.

32. The applicant argues on page 9, 4th paragraph that "the preload circuit of Hammond does not load 'at least one translation of at least one effective address to at least one corresponding real address.'" However, as written in independent claims 1, 12, and 35, the claims state that "translation data" is loaded "for at least one translation..." Nowhere do the identified claims actually state that the loaded data is an actual translation, which is what the applicant is arguing.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck